Monolithic Integration of a Folded Dipole Antenna With a 24-GHz Receiver in SiGe HBT Technology

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***Abstract*—The integration of an on-chip folded dipole antenna with a monolithic 24-GHz receiver manufactured in a 0.8-μm SiGe HBT process is presented. A high-resistivity silicon substrate (1000 $\Omega \cdot$ cm) is used for the implemented circuit to improve the efficiency of the integrated antenna. Crosstalk between the antenna and spiral inductors is analyzed and isolation techniques are described. The receiver, including the receive and an optional transmit antenna, requires a chip area of 4.5 mm^2 and provides 30-dB conversion gain at 24 GHz with a power consumption of 960 mW.**

***Index Terms*—Dipole antennas, heterojunction bipolar transistors (HBTs), monolithic microwave integrated circuit (MMIC) receivers.**

I. Introduction

THE development of monolithic K-band RF frontends in Si/SiGe processes, such as the fully integrated receivers reported in [1] and [2], enables the design of low-cost short-range radar and communication devices for the 24-GHz industrial–scientific–medical (ISM) band. Since all high-frequency components of the receiver, including the low-noise amplifier (LNA), local oscillator (LO), and downconversion mixer, reside on the same chip, no high-frequency interconnects between the building blocks of the receiver are needed. However, the package still has to provide a low-loss high-frequency interconnect to the off-chip antenna. This last off-chip RF interconnect could be removed if the antenna is integrated on the same chip as the rest of the frontend.

On-chip antennas have traditionally been considered for III–V monolithic microwave integrated circuit (MMIC) processes where the high-resistivity substrate with a backside ground-plane metallization can be used for microstrip circuits and patch antennas. In the case of Si/SiGe high-frequency circuits, lumped passive elements are commonly used instead of transmission line components due to the absence of backside metallization, and high losses in the silicon substrate. The use of lumped passive elements also yields comparatively compact circuit layouts (less than 1.5 mm^2 for the receiver reported in [1]), which, in turn, reduces the cost of the manufactured chips. As a small die size precludes the integration of K-band high-directivity antennas, the main requirements for an on-chip antenna are low area consumption and high radiation efficiency in the presence of the silicon substrate. The antenna feed type (balanced or single ended) should preferably match the integrated circuit (IC) topology to avoid the need for baluns.

The half-wave dipole antenna offers a balanced feed, and is thus suitable for integration with differentially designed integrated receivers and transmitters. A 10-GHz on-chip dipole connected to a voltage-controlled oscillator (VCO) has been demonstrated in SiGe HBT technology [3], but poor radiation efficiency (10%) was reported due to high substrate losses. Micromachined meander dipole antennas [4] have been suggested as a way of integrating compact high-efficiency antennas on the low-resistivity wafers commonly used in commercial Si/SiGe bipolar and BiCMOS processes. Micromachining does, however, require additional post processing of the manufactured wafer.

High-resistivity silicon has been proposed as a substrate for millimeter-wave circuits and it has been shown [5] that low-loss microstrip transmission lines can be implemented on such substrates. Monolithic microstrip antenna arrays have been demonstrated at 94 GHz [6], thus validating the use of high-resistivity silicon in antenna applications. The efficiency of monolithic integrated 77-GHz half-wave dipoles manufactured in a commercial active device silicon process has been improved by the use of an undoped silicon substrate placed adjacent to the low-resistivity active device chip [7]. In this case, the high-resistivity silicon was used to guide the waves to an external lens antenna. As an alternative, high-resistivity silicon wafers can be used directly as substrate material in some commercial Si/SiGe foundry processes to enhance the efficiency of an on-chip antenna. In a previous study [8], monolithic integration of simple shorted dipole with a 24-GHz receiver [1] manufactured on a high-resistivity silicon wafer has been demonstrated. However, the implemented antenna was not impedance matched to the integrated receiver and did not utilize the available on-chip space efficiently.

In this paper, we extend the work reported in [8] and provide the results from a full characterization of the 24-GHz receiver where the simple antenna has been replaced with a compact folded dipole, and matched to the input impedance of the

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receiver. Section II presents the characteristics of the selected SiGe HBT process. Section III describes the design of the integrated antenna. Section IV outlines the receiver design. Section V provides details about the utilized on-chip isolation techniques. Section VI then provides the characterization setup and results for the integrated antenna receiver are presented.

II. SiGe HBT Technology

The 24-GHz receiver and the on-chip antenna were designed for the Atmel SiGe2RF [9] process. It is a 0.8-μm Si/SiGe HBT technology with a minimum effective emitter width of 0.5 μm. Metal–insulator–metal (MIM) capacitors, four resistor types, and three metallization layers are available. A selectively implanted collector technique increases the transit frequency f_T from 50 to 80 GHz at the cost of a reduced breakdown voltage (2.4 V instead of 4.3 V). The maximum oscillation frequency f_max is 80 GHz.

High-resistivity silicon substrates (1000 $\Omega \cdot$ cm) are available as a process option in addition to the standard (20 $\Omega \cdot$cm) low-resistivity wafers, thus facilitating the design of on-chip antennas with reduced substrate losses. In this study, 500-μm-thick silicon wafers were used. The surface of the processed silicon substrate is a doped p^+-type to prevent an unwanted inversion layer formation. Normally, the p^+ layer is connected to circuit ground. The locations where this doping should be omitted are marked by the so-called "channel-stopper" layer, which is a negative mask. This mask can be applied for sensitive passive devices such as spiral inductors and antennas in order to reduce the substrate losses.

III. Dipole Antenna Design and Simulation

Integrated antennas offer the possibility of deviation from the standard 50-Ω system impedance in order to allow direct connection of the antenna to the first stage circuits without the need for a matching network. The choice of a suitable antenna impedance for the receiver is governed by the optimum reflection coefficient Γ_opt for minimum noise of the integrated LNA. Noise figure measurements of a standalone version of the receiver LNA suggest a differential optimum antenna impedance of $70 + \mathrm{j}40\ \Omega$.

In previous integration work using this receiver [8], a simple dipole was used, which, due to space constraints, had to be top loaded with lengthening sections perpendicular to the main dipole. However, presence of dielectric materials and conductive bodies close to the dipole radiator tends to lower the radiation resistance, thus causing a significant drop of the antenna impedance at resonance compared to the theoretical free-space value. Shortening the radiator by folding back the ends, as often required due to chip size restrictions, will further decrease the radiation resistance.

Printed folded dipole antennas offer an input impedance, which can be adjusted over a wide range using the design formulas derived by Lampe [10]. The input impedance for a dipole of length L is given as

$$Z_\mathrm{in} = \frac{2(1+a)^2 Z_d Z_x}{(1+a)^2 Z_d + 2Z_x} \tag{1}$$

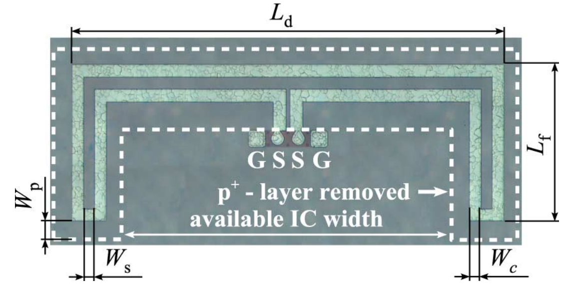

Fig. 1. Chip photograph of the designed folded dipole test structure.

where Z_d is the impedance of the equivalent dipole, Z_x is the impedance of the transmission line mode, and $a = I_1/I_2$ is the ratio of the currents on the driven and parasitic branches of the radiator. The transmission line mode impedance Z_x is obtained as the impedance of a shorted stub (formed by half the dipole)

$$Z_x = jZ_0 \tan(kL/2) \tag{2}$$

where Z_0 is the characteristic impedance and k is the propagation constant of the coplanar strip line (CPS), formed by the driven and parasitic radiator.

For the special case of equal conductor width W_c of the two branches and narrow conductor spacing W_s, the folded dipole yields a impedance step up ratio $(1+a)^2$ of four at resonance (where Z_x goes to infinity) compared to an ordinary half-wave dipole with the same printed conductor dimensions. By folding the on-chip dipole, the antenna impedance can thus be increased to a value closer to Γ_opt of the LNA.

In Fig. 1, a chip photograph of the designed on chip antenna is shown. The antenna was simulated and optimized using Agilent Technologies' High Frequency Structure Simulator (HFSS) [11] full 3-D EM simulation package to account for the reduced effective dielectric constant of the finite dielectric substrate created by the dicing of the wafer into individual chips.

The length of the straight section L_d was limited to 2100 μm as a compromise between chip size and antenna radiation resistance, thus requiring an additional lengthening section $L_f = 750\ \mu$m to be added to each of the radiator ends in order to obtain resonance at 24 GHz. These lengthening sections were added along the edge of the chip, perpendicular to the main radiating section of the dipole, in order to minimize current canceling effects in the far field. The sensitivity of the antenna impedance and efficiency with respect to the conductor width W_c was analyzed by HFSS simulations and found not to be critical. The width $W_c = 60\ \mu$m was selected to keep the resistive losses of the aluminum metallization below the dominant substrate losses, while at the same time minimizing the area requirement for the antenna. A slot width $W_s = 60\ \mu$m, equal to the conductor width, was used between the conductors in the radiator.

The ground clearance W_p, defined as the distance between the radiator metallization and grounded layers such as the p^+ channel stopper or circuit metallization, is an important design parameter as large conductive areas in the vicinity of the antenna will decrease the radiation resistance of the antenna due to induced currents. Based on simulation results, the p^+ channel stopper doping of the substrate was removed within a distance

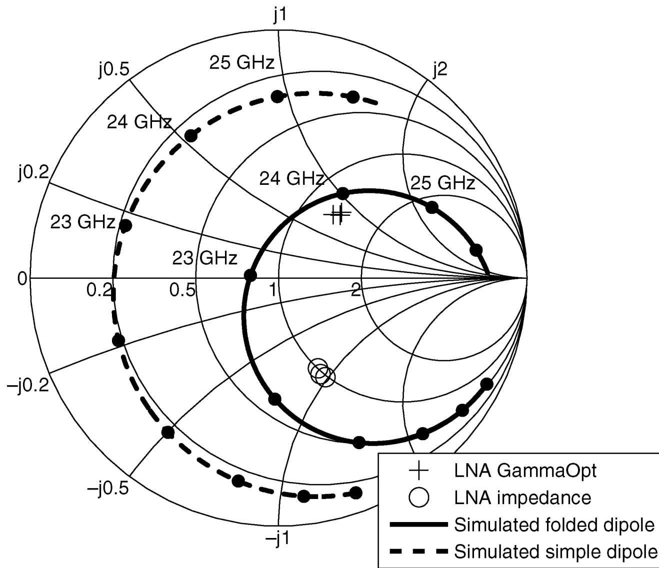

Fig. 2. Simulated antenna impedance of simple (dashed line) and folded dipole (solid line) of the same dimensions with a full 2300 × 2300 μm chip size. Frequency range: 18–26.5 GHz; 1-GHz marker spacing. LNA differential antenna impedance (circles), LNA optimum input reflection coefficient (crosses).

$W_p = 150\ \mu$m of the dipole in order to reduce the losses caused by this low resistive layer.

In the simulation, a substrate thickness of 500 μm and a chip size of 2300 × 2300 μm was used, which corresponds to a distance of 100 μm between the antenna metallization and the edge of the diced substrate. The antenna is operated above its resonant frequency, as shown by the simulated trace in Fig. 2, to provide an inductive impedance close to a conjugate match of the LNA at 24 GHz, which also coincides with $\Gamma_{\rm opt}$. As reference, the simulated impedance for a simple nonfolded dipole of equal dimensions L_d, L_f, and W_c is also shown in this figure. The simulated gain is 1.8 dBi.

IV. Receiver Design

A. Circuit Topology and Passive Elements

In contrast to the backside ground-plane metallization available in III–V MMIC technologies, no ground plane is usually present in Si/SiGe-based technologies, which, in conjunction with high substrate losses, makes a microstrip design approach difficult. A coplanar design has been demonstrated at this frequency with good performance [12]. However, a topology based on distributed elements leads to a drastic increase of size compared to a lumped passive element implementation. Therefore, a design based on lumped elements was chosen in this study. To improve the accuracy of the circuit level simulation, the S-parameters of the inductors were measured on-wafer on separate test structures with the effect of bond pads removed by the use of on-chip deembedding structures.

Due to the lack of a common high-frequency circuit ground plane, it is difficult to define a stable circuit ground. A fully differential design topology has, therefore, been used, which avoids the problem by using 180° phase-shifted signals to provide local virtual ground points at the symmetry axis of the differential circuit. Other advantages of the differential topology

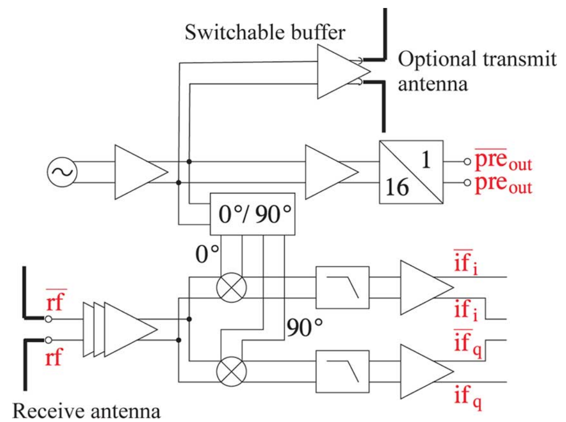

Fig. 3. Block diagram of the integrated receiver, as presented in [8]. The optional transmitter antenna is coupled to the LO through a switchable buffer.

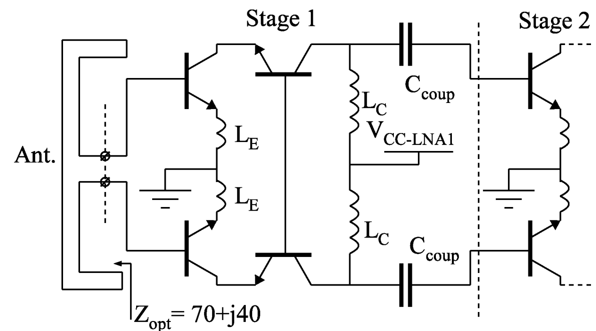

Fig. 4. Simplified schematic circuit diagram of the receiver antenna interface and the first differential cascode amplifier in the three-stage LNA.

are rejection of common-mode noise from supply lines and substrate, increased voltage swing, and suppression of even-order harmonics.

B. 24-GHz Receiver Architecture

The self contained 24-GHz receiver consists of an LNA, a voltage-controlled LO with an output buffer and a quadrature downconversion mixer, as depicted in Fig. 3. The receiver can either be operated at zero IF or as an image reject receiver, but the IF poly-phase filter for a image rejection was not integrated to avoid increasing the chip size unnecessarily. A separately powered 16 : 1 static frequency divider [13] is connected to the output of the VCO to facilitate phase locking of the LO by an external low-frequency phase-locked loop (PLL). At the LO output, a switchable buffer amplifier is also connected in order to allow the chip to be used as a simple frequency modulated transmitter.

The LNA is designed with three stages, each consisting of four transistors in a differential cascode configuration, as shown in Fig. 4. Transistors with 0.8 μm × 20 μm emitter size are used in the cascode, requiring a total dc power of 340 mW for the three stages in the differential configuration. *LC* networks are used for the inter-stage matching, and the 0.13-nH large spiral inductors L_E provide emitter degeneration. For a single-ended standalone version of the LNA, a total gain of 20 dB has been obtained with better than −60-dB reverse isolation (S_{12}). A minimum noise figure of 5.8 dB has been measured, however, 6.6 dB

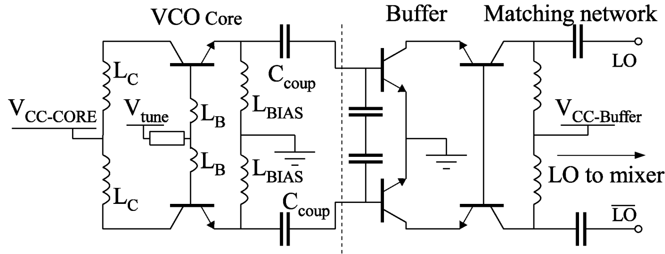

Fig. 5. Schematic circuit diagram of the 24-GHz VCO with integrated buffer amplifier.

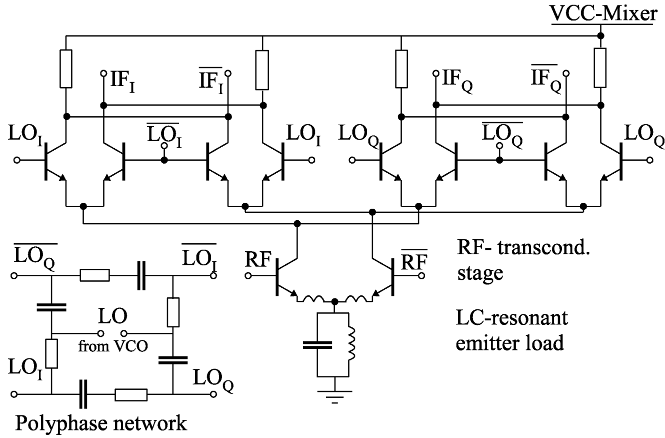

Fig. 6. IQ-downconversion mixer with *LC*-emitter load and polyphase network. The emitter follower IF output buffers are not included.

is expected at the bias point used in the receiver. For the differential version of the LNA, the noise optimum source impedance $Z_{\rm opt}$ is $70 + {\rm j}40\ \Omega$.

A differential common base design is used for the VCO, shown in Fig. 5, where the base inductors $L_B = 0.2$ nH, are used to make the transistors in the oscillator core unstable. Feedback is provided by 0.42-nH large spiral inductors L_C connected to the collectors and the $C_{\rm coup} = 0.11$ pF output coupling capacitors at the emitters. An integrated cascode buffer is used to amplify the output signal. The oscillator–buffer combination has been tested in a standalone configuration where it yields an output power of 7.5 dBm at a center frequency of 23.9 GHz with a dc power requirement is 200 mW. By changing the bias point of the transistors in the core through the $V_{\rm tune}$ control voltage, the VCO can be tuned over a 2.4-GHz range. The estimated phase noise is 80 dBc at 1-MHz offset.

The quadrature downconversion mixer (Fig. 6) consists of two Gilbert switching cores provided with in-phase (I)- and quadrature (Q)-channel LO signals from a conventional single-pole *RC* polyphase network. An input RF transconductance stage is shared by the I and Q mixer cores. A parallel *LC* circuit between the emitters of the stage and ground is used instead of a conventional transistor current mirror to improve the common mode signal rejection of the stage. Emitter followers are used as buffer amplifiers at the output of the mixers. The buffers together with an *RC* low-pass filter are designed to limit the I/Q output signal bandwidth to 470 MHz. The conversion gain of the mixer is designed to be 13 dB and the dc power consumption is 300 mW at a supply voltage level of 4 V.

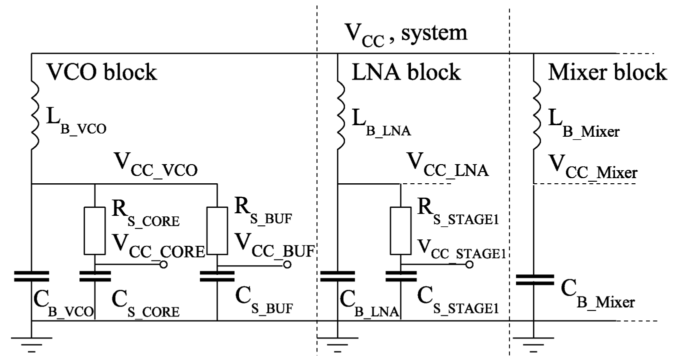

Fig. 7. Schematic of the *LC/RC* filter network for decoupling of the V_{CC} supply line between different receiver blocks and stages [14].

V. Isolation Techniques

Successful single chip integration of a complete receiver with an antenna requires that good isolation can be obtained between stages of the different functional blocks, as well as between the circuit and antenna. Poor isolation can lead to instability and self-oscillation of amplifier stages, noise pickup, increased phase noise of the LO, and saturation or dc-offset problems if the LO signal is picked up by the on-chip antenna.

A. Circuit Isolation

Due to the high integration level, spiral coils are placed in close vicinity. The coupling between these elements has been studied in [14], but due to the weak influence of the evaluated coupling properties on the circuit performance, it can be neglected and the modeling of this effect was not performed. A reduction of the coupling between inductors was obtained by placing a grounded metal ring around these elements, which drastically reduces the crosstalk for a given spacing between these components [15].

The supply voltage lines of the circuit are filtered both at block (such as LNA or VCO) and stage levels, as depicted in Fig. 7.

Different stages within a block, such as the core and the buffer in the VCO, use *RC* filters with the capacitor C_S connected to ground as close as possible to the stage and a resistor R_S connected to the V_{CC} rail of the block.

LC low-pass filters are used to isolate the supply of different blocks sharing the same V_{CC} rail. The inductors L_B are large on-chip inductors with an inductance of 1 nH. The block decoupling capacitors C_B are obtained by connecting several capacitors in parallel, yielding a total capacitance in the decoupling network of approximately 30 pF.

In order to estimate the isolation provided between the supply voltage line of a block and the V_{CC} node of a single stage, a test structure combining both *LC* and *RC* dc-filtering network techniques has been separately manufactured and evaluated [14]. The provided isolation between the two nodes is better than 50 dB between 13–30 GHz.

B. Antenna to Circuit Crosstalk

Crosstalk with the on-chip antenna will primarily appear as common mode components on the differential signal lines of the due to the compact and symmetrical layout of the stages.

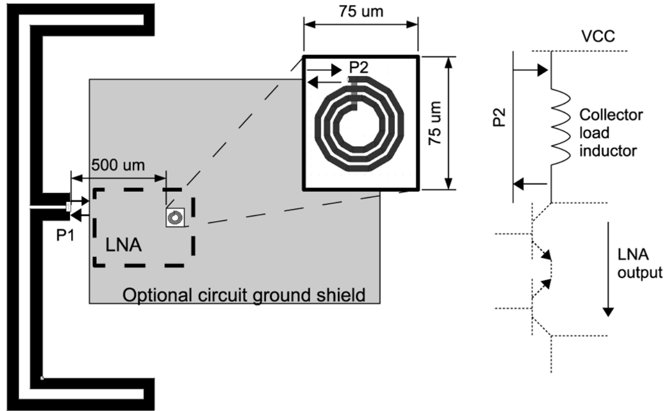

Fig. 8. Crosstalk simulation setup including LNA tank inductor, optional circuit ground shields, and on-chip antenna.

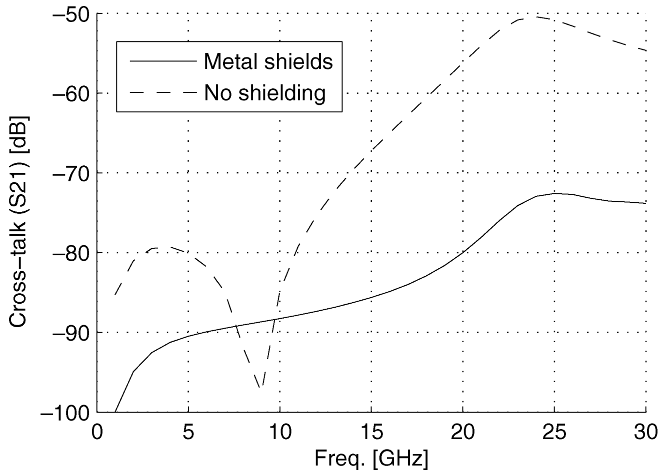

Fig. 9. Simulated crosstalk (solid line with metallic shields, dashed line without) between the on-chip antenna and spiral inductor in the output of the LNA.

However, differential mode crosstalk can appear on signal lines through spiral inductors unless two inductors with opposite winding directions are used in a balanced configuration. The spiral inductors would also need to be closely spaced to prevent any coupling to the antenna from the differential mode components, which is difficult to achieve in practice due to the comparatively large physical size of the inductors.

A critical point for antenna crosstalk is the LNA output matching network. To prevent self-oscillation, larger isolation than the gain of the LNA is needed. The crosstalk between the antenna and a collector load inductor in the output stage of the LNA has been simulated using the method of moments (MoM) package IE3D [16]. An infinite substrate was assumed in the simulation and the complex shaped shielding ground metallization, present in the receiver layout, was replaced by a rectangular shield with an opening for the studied inductor, as shown in Fig. 8.

The simulated coupling between inductors in the collector network of the LNA and the antenna is shown in Fig. 9. The use of grounded metallic shields in the vicinity of the inductors reduce the simulated crosstalk from −51 to −72 dB at the antenna resonance frequency.

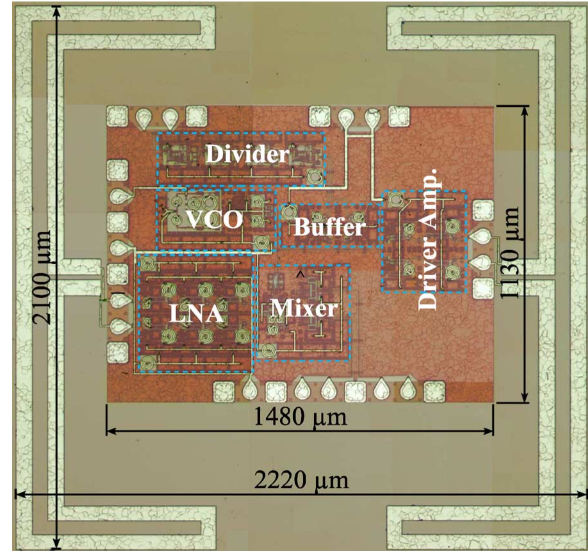

Fig. 10. Manufactured receiver chip with integrated receive antenna (*left*) and auxiliary transmit antenna (*right*).

VI. Implemented Receiver IC

A chip photograph of the manufactured receiver is shown in Fig. 10. The overall system requires an area of $2220 \times 2100\,\mu\text{m}^2$, including the receive and auxiliary transmit antenna.

The simulated coupling between the receive and transmit antenna is −6.5 dBi (free-space conditions), which restricts the use of the simple switchable transmitter stage to half duplex communication.

The circuit part of the 24-GHz integrated antenna receiver requires only $1480 \times 1150\,\mu\text{m}^2$ of the total area, thus leaving space for integration of other circuit blocks such as a PLL, IF signal processing, or upconversion mixers for a transmit path. The receiver circuit was placed in between the two antennas in a region where the channel stopper layer was not omitted. Both the receive and auxiliary antennas are connected to the circuit using short traces. A separate passive antenna chip, identical to one of the integrated antennas without the receiver circuit, was also manufactured on the same wafer to facilitate characterization.

Wafers containing the manufactured receivers and passive antennas were diced before characterization to prevent dielectric loading of the antennas and coupling to nearby circuits on the wafer.

VII. Results and Discussion

A. *Passive Antenna Characterization*

The passive dipole antenna test chip has been characterized in an environment equivalent to free space using a modified wafer probe station [17]. For the antenna impedance measurements, the antenna was supported by a low dielectric constant foam material backed by an absorber, thereby preventing impedance shifts due to dielectric loading and reflections from metallic parts.

The measured and simulated antenna impedance is shown in Fig. 11 for the separately manufactured passive antenna

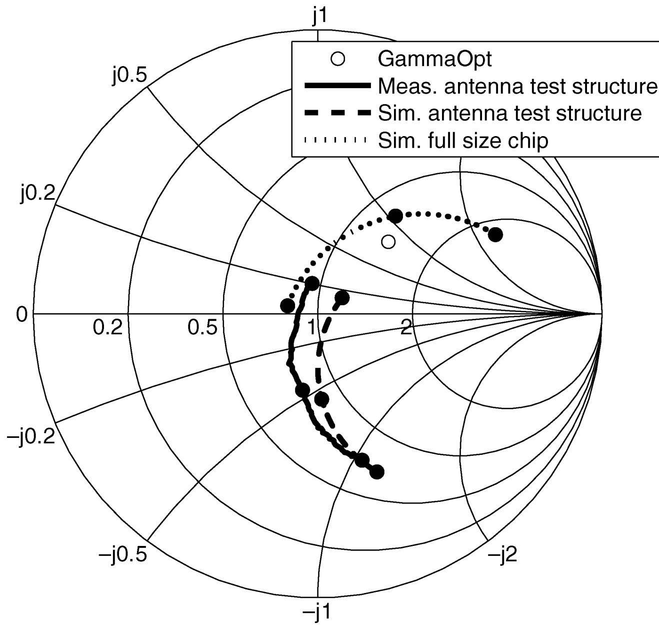

Fig. 11. Measured and simulated antenna impedance: 23–25 GHz. Passive antenna test chip mounted on foam (solid line), HFSS simulation of antenna test chip (dashed line), and HFSS simulation of antenna on receiver chip (dots).

chip, together with the simulated impedance for the full $2300 \times 2300\ \mu\text{m}^2$ large receiver chip.

Good agreement between simulated and measured impedance is obtained over the 23–25-GHz frequency range. The de-tuning of the dipole test structure compared the designed antenna for the full size receiver is caused by the smaller die size and, thus, lower effective dielectric constant of the diced substrate.

Antenna gain and radiation patterns were measured with the antenna under test (AUT) mounted on a foam dielectric in free space. The RF connection to the antenna was provided by a wafer probe. As the probe positioning equipment blocks part of the relatively omnidirectional radiation pattern, the probe setup had to be covered with absorbers to minimize unwanted reflections. The setup was calibrated for gain measurements by replacing the AUT and wafer probe with a 20-dBi standard gain horn antenna.

The measured radiation pattern and gain is shown in Fig. 12 for the passive antenna chip. In the H-plane measurement, the probe setup partly shadows the AUT for negative angles. A front-side gain of -2 dBi is obtained in measurements. The low gain compared to the value obtained in the design can be caused by underestimation of the conductance in the p^+ channel stopper doping used for the initial design, as well as decreased substrate resistivity during processing. Simulations of the antenna test structure with a p^+ layer surface resistivity of $250\ \Omega/\square$, also shown in Fig. 12, yield -3-dBi antenna gain in the same direction, which indicates that a larger p^+ layer clearance is needed to fully take advantage of the high-resistivity substrate. The measured -15-dBi H-plane cross polarization level is higher than the -45-dBi result obtained in the HFSS simulation. However, the increased cross polarization level can be explained by interference from the wafer probe.

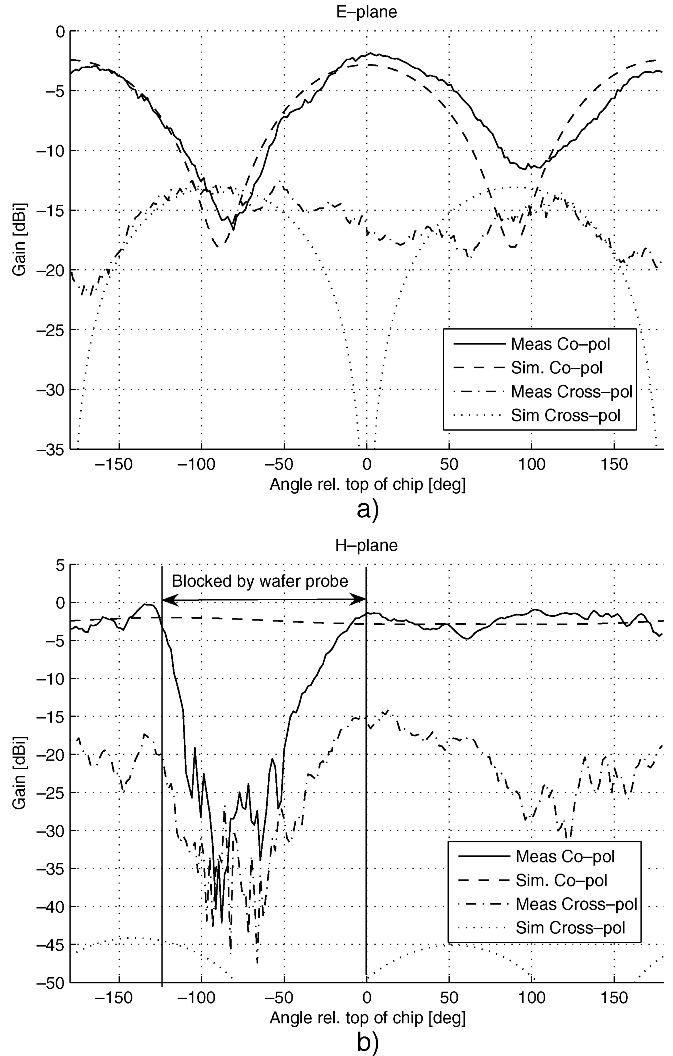

Fig. 12. Measured (co-polarization: solid line; cross polarization: dotted–dashed line) and simulated (co-polarization: dashed line; cross polarization: dots). (a) E- and (b) H-plane radiation pattern and gain of the passive antenna chip.

B. System Characterization

For system characterization, the integrated antenna receiver chip was mounted on a metallic carrier, as shown in Fig. 13, to provide a heat sink for the circuit. A thermal compound was used to enhance the heat transfer from the chip to the carrier. To minimize the loading effect of the metal carrier on the integrated antenna, the chip was mounted with the antenna part of the chip sticking out 1 mm from the edge of the carrier. The electrical connections to the chip were provided with wafer probes. Ground–signal–signal–ground (GSSG) probes were used to extract the I- and Q-channel baseband signal, while the dc power was provided with a needle probe. The overall dc consumption is 960 mW at 4-V supply voltage. The LO signal leakage at the V_{CC} port of the receiver was characterized in a separate setup, where the V_{CC} supply current was supplied through a microwave probe and bias-T. Using a spectrum analyzer, an LO leakage power of -51.5 dBm was recorded, thus verifying good decoupling of the V_{CC} line.

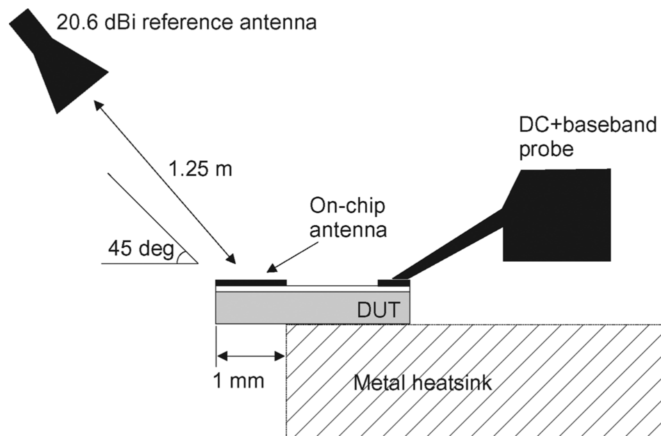

Fig. 13. System noise and conversion gain characterization setup.

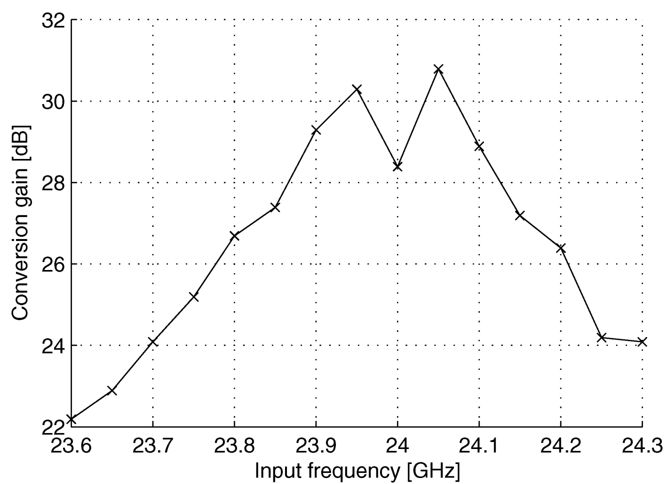

Fig. 14. Measured conversion gain at the I-channel output with illuminated on-chip antenna.

A continuous wave (CW) test signal with a frequency of 24.10 GHz and $P_t = -14.7$ dB power was generated with a synthesized signal generator and applied to a standard gain horn antenna for illumination of the device-under-test. As the gain of the horn is $G_t = 20.6$ dBi at this frequency, an effective isotropic radiated power (EIRP) of $P_t Gt = 5.9$ dB was yielded. The horn antenna was positioned at a distance of 1.25 m from the receiver chip and oriented for maximum received power while the IF output signal was monitored on a spectrum analyzer.

The conversion gain characteristics at a constant LO frequency are depicted in Fig. 14. For a fixed LO frequency of $f_{\rm LO} = 24.07$ GHz, a 3-dB bandwidth of 500 MHz and a maximum conversion gain of 31 dB are obtained. A drop in conversion gain is measured for input signals close to the LO frequency due to the high-pass characteristics of the IF balun used. The receiver input and output 1-dB compression points have not been characterized for the receiver with an integrated antenna; however, for a standalone version, receiver chip $P_{1\ \rm dB,in} = -27.0$ dB and $P_{1\ \rm dB,out} = 5.6$ dB has been reported [1].

The I/Q channel imbalance was measured at a output frequency of 50 MHz, yielding 1.2-dB amplitude error and a phase

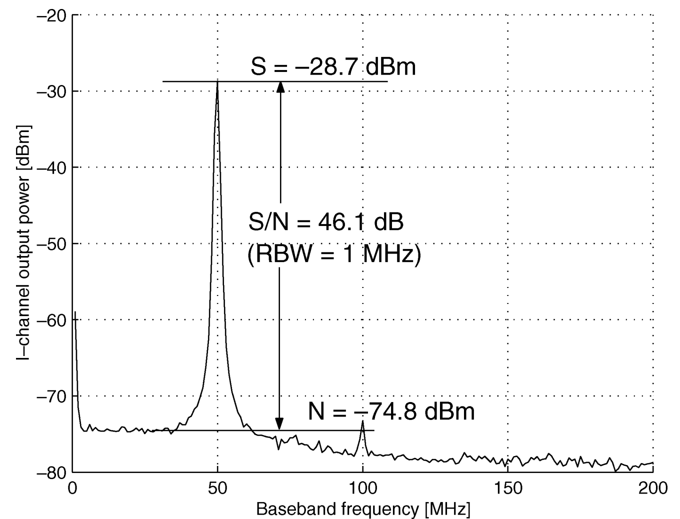

Fig. 15. Measured I-channel baseband output spectrum when illuminated with EIRP 5.9-dBm signal at 1.25-m distance. RBW: 1 MHz; analyzer noise floor: −93 dBm.

imbalance of 4.3°. DC offsets of −47 and −70 mV have been measured at the I and Q baseband outputs. If the dominant cause of the dc offset is assumed to be self-mixing of the 8-dBm strong LO signal generated on chip, the result indicates better than 46-dB isolation between the LO output signal and antenna.

The noise performance of the integrated antenna receiver has been evaluated in the conversion gain setup using the measured power spectrum of the I-channel output, which is shown in Fig. 15.

A signal-to-noise ratio $\mathrm{S/N} = 46.1$ dB is obtained with a 1-MHz resolution bandwidth (RBW). The result corresponds to a signal to noise spectral density $\mathrm{S/N_0} = 106.1$ dB/Hz. Considering an equivalent input signal in an isotropic receiver antenna of −56.1 dBm, as calculated above for the setup, and assuming a background noise floor of −173.9 dBm/Hz at an ambient temperature of 21 °C, a input signal-to-noise spectral density $\mathrm{S/N_0} = 117.8$ dB/Hz is obtained. A single-sideband system noise figure for the receiver including the integrated antenna can thus be calculated as $\mathrm{NF} = 117.8 - 106.1 = 11.7$ dB. If image rejection is obtained through the use of a 90° IF hybrid or processing of the quadrature outputs in a zero-IF application, a double-sideband (DSB) noise figure of 8.7 dB can be obtained. The result is in agreement with the separately measured 6.6-dB noise figure for the LNA and −2-dBi gain for the antenna. Although the measured system noise figure is affected by the measurement setup, as reflections from the heat sink can increase the gain of the antenna and, thus, lower the apparent noise figure in the measurement, the result indicates low pickup of substrate noise by the antenna.

VIII. CONCLUSION

Monolithic integration of a compact folded dipole antenna on the same chip as a 24-GHz receiver manufactured using high-resistivity silicon wafers in a commercial SiGe HBT process has been demonstrated. The implemented radiator requires a $2.1 \times 0.9\ \mathrm{mm}^2$ chip area and provides −2-dBi gain with an impedance level suitable for direct connection of the receiver LNA.

The system performance of the integrated receiver has been evaluated with a maximum conversion gain of 31 dB and a system noise figure of 8.8 dB obtained for the full system including the on-chip antenna. The noise performance of the receiver is in agreement with the theoretical value calculated from the measured antenna gain and LNA noise figure, thus showing that the performance is not significantly degraded by substrate noise.

Isolation techniques, consisting of ground shields around the spiral inductors and *RC*/*LC* filtered dc supply lines, have been used to reduce the amount crosstalk. No instability of the receiver is observed despite the close integration of the antenna and the high-gain LNA. The low dc offsets measured at the I/Q signal output indicates that sufficient isolation between the LO and antenna can be obtained on-chip.

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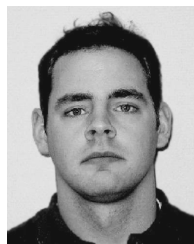

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